

Workshop on Ferromagnetic devices, Circuits and applications

Place: CNSI Building 114 (Auditorium), UCLA, Los Angeles
Date: 21st February, 2008

Workshop Background

The "Workshop on Ferromagnetic Devices, Circuits and Applications" is planned to be a 1 day workshop that will bring together the most renowned scientists from academia and industry working in the space of new ferromagnetic based devices and circuits. Over the last several years, several organized research efforts have focused on use of spin and collective magnetic effects for logic applications. Many device concepts have been proposed, a number have been simulated but few have been fabricated and demonstrated for their logic applications. Up to now, the devices and interconnect mechanisms have been so poorly defined that any meaningful performance estimates of assembled circuits performing useful information process tasks have not been attempted.

Much of the recent research activity on logic spin devices has been driven by the semiconductor industry (Intel and WIN sponsors) as it is directly motivated by potential applications of the new technologies to commercially relevant products. DARPA and other government agencies are motivated by similar interests in potential military and high performance applications. Those two drivers require development of meaningful metrics to mark where the research efforts are and to define future progress toward application goals that may extend beyond general purpose Boolean Logic. The starting point of the workshop would be to review recent results of magnetic devices and interconnects with a focus on experimental results as much as possible and their possible circuit configurations. Consideration of the unique response functions of magnetic devices to external fields and how those responses could be used to process information lies at the heart of this. The final step would be to extract a set of scalar values that parameterize the efficiency of the information processing and call those the metrics.

Workshop Output

The outcome of the workshop will result in a summary paper composed by each session chair that most likely will be incorporated into the International Technology Roadmap on Semiconductors (ITRS) or may stand as a single paper in its own right.

Speaker Expectations and Questions to Answered

- a) What will spin logic devices look like in 5 years, 10 years and beyond?
- b) What experiments would be required to demonstrate their function?
- c) Do materials (systems) exist to support these devices? Or is additional material research required?
- d) What performance benefits are expected? (power, speed, functionality)
- e) How will they be interconnected to perform information processing?
- f) What key learning from memory can we take for spin logic? (particularly directed towards industry)
- g) Other implications to be considered include: Si compatibility, manufacturability, variability and others. Any show stoppers here?

DRAFT AGENDA ONLY

Day 1: 21st February, 2008

8:00 - 8:30 a.m.	LIGHT BREAKFAST + REGISTRATION
	Opening Remarks – Kang L Wang (WIN) George Bourianoff (Intel)
Focus Topic 1: Commercialized Magnetic/Spin Devices by Industry	
8.45 – 9.20	Freescale – Nick Rizzo (confirmed)
9:20 – 10:00	Toshiba - Dr. Hiroaki Yoda (confirmed) "Perpendicular MTJ for high density MRAM"
10:00 - 10:30	BREAK
10:30 – 11:10	IMEC - Wim Van Roy (confirmed) "Spin transistors at practical operating conditions"
11:10 – 11:30	Chair led discussion
Focus Topic 2: Ferromagnetic Device and Concepts	
11:30– 12:10	Mark Johnson (NRL) (confirmed) "Perspectives on Magnetoelectronic Logic"
12:10-1:00 p.m.	LUNCH
1:00 – 1:40	Masaaki Tanaka (University of Tokyo, Japan) (confirmed) "Spin MOSFETs and reconfigurable logic design"
1:40 – 2:20	Wolfgang Porod (Notre Dame) - MQCA's (confirmed) "Magnetic Logic based on Field-Coupled Nanomagnets"
2.20 – 2.45	Chair led discussion
3.00-3.15	BREAK
Focus Topic 3: Ferromagnetic Circuits and Interconnection Concepts	
3.20-4.00	Nicholas P. Carter (UIUC) (confirmed) "Reconfigurable Magnetoelectronic Circuits for Threshold Logic"
4:00 – 4:40	Lu Jeu SHAM (UCSD) – "Spin Accumulation Device Concepts" (confirmed)
4:40 – 5:20	Alex Khitun (UCLA) – "Spin Wave based Circuits and Logic" (confirmed)
5:20 – 5:45	Chair led discussion
6:00 p.m.	Dinner