



**“Linking Spin Devices”**  
**WIN Workshop #2**  
*November 15<sup>th</sup> @ Stanford University*  
**Stanford Campus, CIS Building Extension, Room 338**

**Objective:** Critical evaluation of WIN devices and linkage to WIN Circuits and Benchmarking

**Attendees:** All logic device PI's Circuits PI's and Benchmarks

**Chairman :-** Vwani Roychowdhury/Eli Yablonovitch/Jan Rabaey

**Agenda**

2.00	Opening Remarks – Kang Wang
2.05	WIN Integration - Vision and Status – Ajey
2.10	Fundamentals of Integrated circuits – Benchmarks Overview – Mark Rodwell
2.25	Spin FET/SPIN Valve Peidong Yang (10 min) K. L. Wang (10 min) Shan Wang (10 min) J. Harris (10 min) 20 min discussion
3.30	Spin Hall Device D. Awschalom - 10 min/ 20 min discussion
4.00	Spin resonator A. Cleland – 10 min/ 10 min discussion
4.20	<b>Coffee Break</b>
4.40	MQCA Low power logic Jeff Bokor - – 10 min/ 20 min discussion
5.10	Spin Waves Alex Khitun (10 min) Jim Allen (10 min) 20 min discussion
5.50	Spin Torque HongWen Jiang (10 min) 10 min discussion
6.10	Multiferroics Joe Oren/Joel Moore (10 min) 10 min discussion
6.30	Spin Current amplifier Joachim Stohr - Yves Acremann (10 min) 10 min discussion
7.00	<b>DINNER</b>

## **Background and Setting-the-Stage for the 2<sup>nd</sup> WIN Workshop**

There are several spintronic logic devices being explored within WIN, all with intentions to replace the current CMOS technology. Individual CMOS devices would become difficult to be scaled beyond 15 nm technology (2020) node because of various disordered mechanisms including [quantum mechanical and manufacturing limits](#). This opens up opportunities to explore novel devices. However, an alternate technology requires a thorough understanding and comparison to the current logic devices.

The technology contender has to be compared with various fundamental parameters the two most important items being 1) Throughput and 2) power consumption/dissipation. Apart from these classical limits, other concepts to be considered by the “next” technology are 1) Manufacturability, scalability and compactness (size per bit function) 2) Fundamental limits such as quantum, thermodynamic and electromagnetic 3) feasibility of information transfer (interconnect) which is associated with device fan out and gain ability.

In addition, some questions to be addressed by to the devices are:

1. What is the principle of switching?
2. How is the device modulated (turn on and off)? (via current? Spin current? Magnetic field? Etc.....)
3. What is the switching speed of the device?
4. What function does the device provide (logic/memory or both?)
5. What is the size of the smallest functional device?
6. How many individual functional devices are required to make a logic function?
7. What are some manufacturing hurdles foreseeable?
8. Can the device be scaled?
9. What is the limiting factor to scaling (i.e. Debye length, tunneling, etc...)
10. How are devices interconnected?
11. Can the device produce gain?
12. Can the device be fanned-out to other devices?
13. What is the power dissipated by the functional device?
14. Is cross talk a problem with the device amongst other neighboring devices?
15. What are the associated leakage mechanisms, if any?
16. Can the device be integrated on a Si platform (using existing CMOS methods)?
17. Does the device operate at room temperature?
18. What is the limiting factor to maximum temperature of operation (i.e. Curie, tunneling, etc...)?

## LOGISTICS


Lodging:

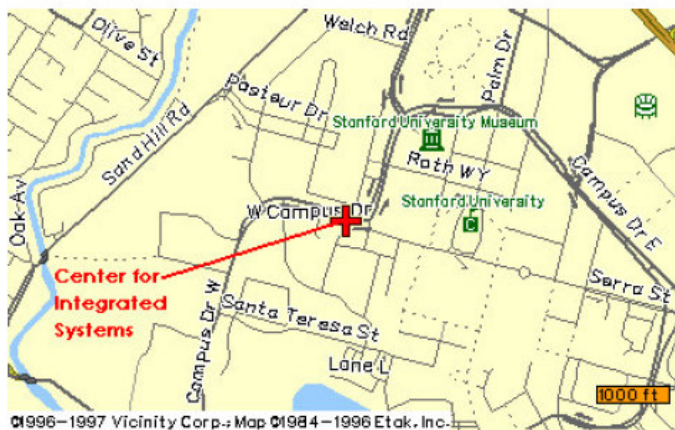
<http://www.stanford.edu/dept/hds/chs/general/hotel.html>

Parking:

Word from Stanford is that parking can be a problem so attendees should check with the hotel regarding the availability of a hotel shuttle or the Marguerite (Stanford) shuttle. Otherwise, there are parking meters for visitors that take 5 quarters per hour, and there are parking passes available for purchase at \$12/day.

## DRIVING DIRECTIONS

 Directions



The Center for Integrated Systems is located at Stanford University on the corner of Campus Drive and Via Ortega. Driving directions to CIS can be found below. The mailing address is:

Center for Integrated Systems  
420 Via Palou  
MS 4070  
Stanford, CA 94305-4070

Stanford's detailed, [searchable campus map](#) can be helpful in orienting yourself to the campus. After linking to the map, scroll down for the keyword search interface, or zoom in and out by clicking on the map itself.

Additional information about visiting Stanford, including public transportation tips, can be found on the [Stanford University visitors site](#)..

a large green utility plant.

7. Parking structure on the corner of Panama and Via Ortega has pay visitor parking on the first floor as you enter from Via Ortega. (\$1.50 an hour, free after 4:00 p.m.)

**From I-280 South:**

1. Exit Page Mill Road & turn right (east) onto Page Mill Road.
2. Turn left at 2nd traffic light onto Junipero Serra Blvd.
3. Turn right at golf course (3rd traffic light) onto Campus Drive West.
4. Turn right onto Panama St.
5. Turn left at Via Ortega.
6. CIS is on the right just after the stop sign, across from a large green utility plant.
7. Parking structure on the corner of Panama and Via Ortega has pay visitor parking on the first floor as you enter from Via Ortega. (\$1.50 an hour, free after 4:00 p.m.)

**From 101 South or North:**

1. Exit Embarcadero Road West.
2. Follow Embarcadero Road to El Camino.
3. Cross El Camino; road name changes to Galvez St.
4. Bear left on Galvez at the stadium.
5. Turn right onto Campus Drive at the stop sign.
6. Go 0.8 miles on Campus Drive; then turn left at Via Ortega, just past the Medical Center.
7. CIS is immediately on the left, at the stop sign.
8. Parking structure ahead and on the right has pay visitor parking on the first floor as you enter from Via Ortega. (\$1.50 an hour, free after 4:00 p.m.)

To ask about special parking arrangements if you are a sponsor, please contact **Maureen Rochford** or **Carmen Mirafior**.

For additional directions or information, please contact [coordinator@cis.stanford.edu](mailto:coordinator@cis.stanford.edu).

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